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Reference


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Double-gated graphene-based devices

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Abstract. We discuss transport through double-gated single- and few-layer graphene devices. This kind of device configuration has been used to investigate the modulation of the energy band structure through the application of an external perpendicular electric field, a unique property of few-layer graphene systems. Here we discuss technological details that are important for the fabrication of top-gated structures, based on electron-gun evaporation of SiO\textsubscript{2}. We perform a statistical study that demonstrates how—contrary to expectations—the breakdown field of electron-gun evaporated thin SiO\textsubscript{2} films is comparable to that of thermally grown oxide layers. We find that a high breakdown field can be achieved in evaporated SiO\textsubscript{2} only if the oxide deposition is directly followed by metallization of the top electrodes, without exposure of the SiO\textsubscript{2} layer to air.

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1. Introduction

The ability to isolate and embed single- and multi-layer graphene in double-gated structures is paving the way to reveal the unique electronic properties of these systems [1]–[13]. Independent voltages applied to a nano-fabricated top gate and to the back gate offer the possibility to gain local control of the charge density and to impose locally a perpendicular electric field. This device configuration was used recently to show how the band structure of graphene-based materials can be tuned continuously [8, 12]. In particular, bilayer graphene exhibits an electric field-induced insulating state due to the opening of a gap between the valence and conduction bands [8], and in trilayers, which are semi-metals, the band overlap can be increased substantially [12]. Cleverly designed top gates on a graphene single layer have also been used successfully for engineering p–n junctions [1]–[7], necessary for the investigation of Klein tunneling [1, 3, 4], and to attempt the fabrication of controlled quantum dots [15, 16]. Key to the fabrication of top-gated structures is the ability to deposit good quality thin gate oxides, with high breakdown field and low leakage current. Here, after reviewing the relevance of double-gated devices on the electric field modulation of the band structure of double- and triple-layer graphene, we discuss in some detail technological aspects related to the properties of the SiO$_2$ layers used as gate insulators. In particular, we discuss how we can routinely achieve high breakdown fields in electron-gun evaporated thin SiO$_2$ films (15 nm), comparable to the breakdown fields of thermally grown SiO$_2$, which is surprising given that SiO$_2$ deposited by evaporation was long believed to be a poor quality insulator. To unveil the reasons behind the good insulating quality of our evaporated SiO$_2$ films, we conducted a statistical study of leakage current and breakdown voltage in capacitors, where two metallic electrodes are separated by a SiO$_2$ layer fabricated in different ways. We demonstrate that if SiO$_2$ and top gate metal electrodes are deposited subsequently without exposing the SiO$_2$ to air, the electrical performance of electron-gun evaporated SiO$_2$ is comparable to that of thermally grown SiO$_2$. In contrast, exposure to air of the SiO$_2$ layer before deposition of the counter-electrode leads to much worse insulating characteristics. Our findings indicate that extrinsic degradation—probably due to the absorption of humidity—has limited the insulating quality of electron-gun evaporated SiO$_2$ in the past.

2. Device and fabrication

Single- and few-layer graphene flakes used for the device fabrication were obtained by micromechanical cleavage of natural graphite crystals, and by their subsequent transfer onto a highly
Figure 1. Panel (a) shows a plot of relative green shift (as defined in the main text) for 90 few-layer graphene areas, showing clear plateaus for graphene layers of different thicknesses. Panel (b) shows the conductance of a device (indicated by the blue dot in the plot shown in panel (a)) measured in the presence of high magnetic field ($B = 8$ T); plateaus are observed at conductance values characteristic for Dirac electrons, indicating that flakes with relative green shift $= 0.06$ are indeed single layers. Panel (c) shows a schematic representation of double-gated graphene devices, together with the measurement configuration used to study transport as a function of voltages applied to the top and back gates. Panels (d)–(f) show plots of the square resistance in single (d), double (e) and triple (f) layers, respectively, measured while sweeping the top gate, for different fixed voltages applied on the back gate (for single layer $T = 300$ mK, $W = 2$ $\mu$m, $L = 1.4$ $\mu$m, $\mu = 3500$ cm$^2$ V$^{-1}$ s$^{-1}$, double layer $T = 300$ mK, $W = 1.7\mu$m, $L = 1$ $\mu$m, $\mu = 900$ cm$^2$ V$^{-1}$ s$^{-1}$ and for triple layer $T = 1.5$ K, $W = 1$ $\mu$m, $L = 1.4$ $\mu$m, $\mu = 800$ cm$^2$ V$^{-1}$ s$^{-1}$).

doped silicon substrate (acting as a gate) covered by a 285 nm thick thermally grown SiO$_2$ layer. The thickness of the graphene layers can be simply identified by analyzing the shift in intensity in the RGB green channel relative to the substrate (i.e. relative green shift) [8, 12, 14, 17, 18]. A plot of the relative green shift, as extracted from optical microscope images of various samples taken with a digital camera, exhibits plateaus corresponding to the discrete thickness values—see figure 1(a). Subsequent transport measurements (quantum Hall effect, resistance dependence on a perpendicular electric field, etc) confirm the validity of this optical method (figure 1(b)). The fabrication of nanostructures is accomplished by conventional electron-beam lithography. Metallic contacts and top gates were deposited by electron-gun evaporation, respectively, of Ti/Au (10/25 nm thick with a background pressure of $9 \times 10^{-7}$ Torr) for contacts
and SiO$_2$/Ti/Au (15/10/25 nm thick with a background pressure of 3 × 10$^{-7}$ Torr) for top gates, followed by lift-off. We took special care to fabricate all the ohmic contacts within 60 nm from the edges of the top-gated areas, so that two probe resistance measurements are dominated by the resistance of the double-gated region [19]. All transport measurements in double-gated devices (see figure 1(c)) were made using a lock-in technique (excitation frequency: 19.3 Hz), in the linear transport regime, at temperatures ranging from 300 mK up to 150 K.

To understand why, contrary to expectations, we manage to achieve high breakdown field in thin, electron-beam evaporated SiO$_2$ films, we conducted a macroscopic study of the breakdown characteristics on two types of capacitor test structures. The first—which we refer to as type A—is characterized by subsequent evaporation of SiO$_2$/Ti/Au without breaking the vacuum in between the deposition of the different materials. For the second—type B SiO$_2$—we exposed the device to ambient for 1 h after the SiO$_2$ deposition, before evaporating the Ti/Au counter-electrode. The breakdown test measurements were made with a Keithley-2400 source-meter on more than 130 different capacitors (with three different surface areas: 125 × 115, 175 × 150 and 215 × 195 µm$^2$).

3. Transport experiments in double-gated few layer graphene devices

The measurement configuration used for double-gated devices is shown in figure 1(c). A finite voltage applied to either one of the gates (back or top gate) changes the position of the Fermi level in the corresponding gated region of the graphene layer, by an amount corresponding to the induced charge density. In addition, by biasing the two gate electrodes with opposite polarity, a large external electric field applied perpendicular to the layer is generated, which is equal to $E_{\text{ex}} = (V_{\text{bg}} - V_{\text{tg}})/d_{\text{tot}}$ ($d_{\text{tot}} = 15 + 285$ nm is the total SiO$_2$ thickness). In this device configuration, we can monitor the evolution of the in-plane transport properties for each few-layer graphene device as a function of $E_{\text{ex}}$. Figures 1(d)–(f) show the typical behavior of the square resistance measured, respectively, in double-gated single- (d), double- (e) and triple- (f) layer graphene, when sweeping the top gate, while keeping the back gate at a fixed potential. It is apparent that the overall electric field dependence of $R_{\text{sq}}$ is markedly distinct for graphene layers of different thicknesses. In all cases, the resistance exhibits a maximum ($R_{\text{sq}}^{\text{max}}$) whose value and position in gate voltage depend on the voltage applied to the gate on which a fixed potential is applied during the measurement. At $E_{\text{ex}} = 0$ V m$^{-1}$ we find that for single- and bilayer graphene $R_{\text{sq}}^{\text{max}} \sim 6$ KΩ, close to a conductance per square of $4e^2h^{-1}$, as expected, indicating that the fabrication of top gate structures does not damage significantly the material (for trilayers the square resistance is somewhat lower, owing to the presence of an overlap between valence and conduction band). Increasing the external electric field induces a well-defined—and different—response for the square resistance of layers of different thicknesses. Respectively, in a single layer, $R_{\text{sq}}^{\text{max}}$ is not affected by a finite $E_{\text{ex}}$; in bilayers at low temperature $R_{\text{sq}}^{\text{max}}$ increases from 6 KΩ to very large values (>100 KΩ); in trilayers $R_{\text{sq}}^{\text{max}}$ decreases with increasing $E_{\text{ex}}$. These experimental findings, confirmed in a number of different samples (three single layers, over ten double and ten triple layers) provide a clear indication that each few-layer graphene is a unique material system, with distinct electronic properties.

6 These measurements on double-gated devices were mainly carried out in a two terminal configuration. Measurements in a four terminal configuration confirmed that the influence of contact resistance present in two terminal devices did not influence significantly the results (see supplementary online information of [12] and [19]).
Figure 2. Panels (a) and (c) show plots of the square resistance at different temperatures for the bilayer and trilayer devices whose data are shown in panel (e) and (f) of figure 1. Panel (b) shows a plot of $R_{sq}$ versus $T$ and $\ln(R_{sq})$ versus $T^{1/3}$ extracted from the measurements shown in panel (a), at $V_{bg} = -50$ V and different $V_{tg}$ values as indicated in the legend. The external electric fields applied on the bilayer for each different $V_{tg}$ are, respectively, $-0.177$ V nm$^{-1}$ (■), $-0.175$ V nm$^{-1}$ (▲), $-0.173$ V nm$^{-1}$ (●), $-0.167$ V nm$^{-1}$ (▲), $-0.16$ V nm$^{-1}$ (▼), $-0.153$ V nm$^{-1}$ (◀). Panel (d) shows the normalized charge density as a function of temperature, extracted from the trilayer measurements of panel (c). The continuous line is a fit based on a two band model with finite overlap (see main text).

Transport measurements over a wide range of temperatures (from 300 mK up to 150 K) underline the unique electronic properties of these few-layer graphene devices. In bilayer graphene the larger $E_{ex}$, the more pronounced is the temperature dependence of $R_{sq}^{max}$, see figures 2(a) and (b). At $E_{ex} = 0$ V m$^{-1}$, $R_{sq}^{max}$ is only weakly temperature dependent (as is typical of zero-gap semiconductors), and at $E_{ex} \neq 0$ V m$^{-1}$ the observed behavior is that typical of an insulating state. In contrast, trilayer graphene devices display a decrease of $R_{sq}^{max}$
when lowering the temperature, stemming from the semimetallic nature of the constituent material.

At a more quantitative level we find that $R_{sq}^{\text{max}}$ in bilayer graphene is well described by $\alpha \exp\left(\frac{T_0}{T}\right)^{1/3}$, with $T_0 \approx 20$ K at the maximum applied external electric field (see inset in figure 2(b)). This temperature dependence is indicative of variable-range hopping in a two-dimensional material where an energy gap has opened, and where disorder causes the presence of sub-gap states ($T_0$ is related to this sub-gap density of states [8])—making it difficult to estimate $\Delta$ from transport experiments.

Indeed, in a disorder free bilayer graphene, at $E_{\text{ex}} \neq 0$ a gap ($\Delta$) opens in the band structure and the density of states in the gapped region is zero. In this ideal case, when the Fermi level is in the middle of the gapped region the value of $R_{sq}^{\text{max}}$ at a finite temperature is entirely determined by thermally activated charge carriers ($R_{sq}^{\text{max}} \propto \exp(\Delta/2k_BT)$). Therefore, $\Delta$ can be accurately determined from a plot of $\ln(R_{sq}^{\text{max}})$ versus $1/T$. On the other hand, in real devices the presence of disorder creates a finite density of states in the band gap of bilayer graphene. Now charge carriers can conduct via variable-range hopping at $R_{sq}^{\text{max}}$. In this case, $R_{sq}^{\text{max}}$ is a function of the density of states at the Fermi level and not any more simply a function of $\Delta$.

The fact that a gap opens in the band structure of bilayer graphene at finite $E_{\text{ex}}$ is evident from the temperature dependence of $R_{sq}$ as a function of charge density. In particular, when the Fermi level lays deep into the conduction and/or valence band, a temperature independent $R_{sq}$ is expected. However, when the Fermi level is shifted across the energy gap region $R_{sq}$ should display an insulating temperature-dependent behavior. Experimentally, this is achieved by measuring $R_{sq}$ at a fixed value of either of the gates (e.g. $V_{bg}$) and for different voltage applied on the other gate (e.g. $V_{tg}$) (see figures 2(a) and (b)). The cross over from band transport to variable-range hopping in the gap occurs at the edge of the valence and conduction band (see figure 2(b)).

Similar previous transport experiments in double gated bilayer [8] reported an energy scale of 1–10 mV associated with the insulating state induced by $E_{\text{ex}} \neq 0$. This energy scale seen in transport is much smaller than the energy gap recently probed in optical spectroscopy experiments ($\Delta \sim 200$ mV at $E_{\text{ex}} = 2$ V nm$^{-1}$ [22]). Possibly the finite sub-gap density of states induced by the disorder is at the origin of the small energy scale measured in transport experiments, however the specific mechanism responsible for these experimental observations remains an open question.

The temperature dependence of the resistance in trilayer graphene is opposite to the one observed in bilayers, and it reveals that this material system is a semimetal with a finite overlap ($\delta \varepsilon$) between conduction and valence band. This band overlap can be estimated within a two band model [12, 20, 21], where the number of thermally excited carriers increases with temperature according to $n(T) = (16\pi m^*/\hbar^2c)k_BT \ln(1 + e^{\delta \varepsilon/2k_BT})$ (where $m^*$ is the effective mass and $c$ is equal to twice the layer spacing). Measurements at finite $E_{\text{ex}}$ show that $\delta \varepsilon$ decreases when increasing external electric field ($\delta \varepsilon$ goes from 32 to 52 meV in the measurements of figure 2(d)).

These experiments demonstrate that a perpendicular electric field applied on few layer graphene is a valuable tool to change the band structure of these materials. Double-gated structures lead to the discovery of the only known electric field tunable insulator, i.e. bilayer graphene, and of the only known electric field tunable semimetal, i.e. trilayer graphene.
4. Evaporated silicon oxide as top gate dielectric

The opening of a sizeable band gap in bilayer graphene, and large changes in the band overlap of graphene trilayers require the application of large external electric fields to these material systems. It is the breakdown field of the gate dielectric that imposes a limit on the maximum value of $E_{ex}$ experimentally accessible in double-gated structures. To optimize this aspect of the devices, we conducted a systematic study of the breakdown electric field of SiO$_2$ gate oxide for devices with different areas, fabricated under different conditions. Here we discuss the details of this investigation. From our statistical analysis, we conclude that what is crucial is not the SiO$_2$ deposition method, but the details in the metallization of top gate electrodes afterwards, which affect the final quality of the oxide gate dielectric.

We compare capacitor devices fabricated following two different procedures for the oxide dielectric/top metal electrode interface. In particular, the devices were fabricated on a Si/SiO$_2$ substrate (identical to the one used for the graphene devices previously described) on which we deposit a Ti/Au (5/20 nm) film—a common electrode for the capacitors. In devices of type A, the SiO$_2$ deposition and top electrode (Ti/Au : 5/20 nm) metallization processes were carried out without breaking the vacuum. In contrast, in devices of type B, the SiO$_2$ gate dielectric was exposed to air for 1 h prior to the deposition of the top electrode metals. The SiO$_2$ deposition was carried out typically at $3 \times 10^{-7}$ Torr back ground pressures. We did not observe a dependence of the insulating properties of the SiO$_2$ dielectric, breakdown field and leakage current over the background pressure range from $1 \times 10^{-7}$ to $5 \times 10^{-7}$ Torr.

Figures 3(a) and (b) show various $I-V$ traces, measured in ambient condition, for type A and type B devices. A first clear difference between the two types of devices is the magnitude of the leakage current, visible by plotting the $I-V$ curves both in linear and logarithmic scale, see figure 3. For a surface area of $215 \times 195 \mu m^2$, we find $I_{leakage} \simeq 2.5 \times 10^{-10} A \mu m^{-2}$ for the best type B devices which is one order of magnitude larger than that measured in the worst type A devices (the differences for typical devices are much larger than one order of magnitude). This extremely different level of leakage current already indicates that the exposure of SiO$_2$ to air prior to the deposition of top metals has a large negative influence on the insulating performance of the oxide.

The $I-V$ characteristics further show that for a fixed surface area ($215 \times 195 \mu m^2$), the breakdown voltage $V_{BD}$ for type A is typically in the range $8 V < V_{BD} < 9 V$ whereas type B devices break down anywhere in the range $0 V < V_{BD} < 6 V$. The differences in the failure of device types are best summarized in the histogram plots of $V_{BD}$—see figure 4(a). For type B we find a large spread in the distribution of $V_{BD}$, in contrast to the narrow distribution characteristic of type A devices. Furthermore, the comparison of $V_{BD}$ for type A devices with different surface areas shows that $V_{BD}$ increases with decreasing device area, possibly indicating that the properties of SiO$_2$ in type A close to breakdown are determined by small defects present in the film with rather small probability. Consistently, we observe that the leakage currents of these devices at low bias exhibit only small sample-to-sample fluctuations, suggesting that the SiO$_2$ layers in type A devices are very uniform.

To try to quantify our observations better and analyze the role played by the specific fabrication technique and surface area on the device performance (e.g. breakdown field), we adopt a failure analysis methodology [24]. In what follows, we provide a statistical description of the breakdown probability introducing the cumulative probability ($P$) as the probability of a device breaking down at a given voltage. From failure methodology, we notice that
possibly the most flexible distribution for the failure of a population of samples is the Weibull distribution \([24, 25]\) \(P = 1 - \exp \left[ - \frac{V_{BD}}{V_0} \beta \frac{S}{S_0} \right]\) (where \(S\) is the capacitor surface area, \(S_0\) is the reference surface area, \(\beta\) and \(V_0\) are the Weibull parameters). The parameter \(\beta\), also known as the Weibull shape parameter, determines the shape of the probability density function, i.e. higher \(\beta\) indicates distributions with low dispersion of \(V_{BD}\).

\(V_0\) is the Weibull scale parameter, whose only effect is to scale the \(V_{BD}\) distribution (the larger \(V_0\), the more ‘stretched’ the distribution). Depending on the value of the Weibull parameters, this distribution mimics the behavior of other statistical distributions such as the normal and the exponential. Given a sample population, the Weibull parameters provide a quantitative measure of the failure probability. Both \(\beta\) and \(V_0\) are strongly affected by the failure mechanism which can eventually be identified when comparing the Weibull parameters for different sample populations. For instance, a value of \(\beta\) that does not depend on the capacitor surface area—i.e. the variance does not change with the surface area—means that the microscopic mechanism of breakdown is common to all the samples, independent of the specific area \([25]\).

The good agreement between a fit to the Weibull distribution of the cumulative probability for each different surface area and device type shows that the data of each different device population is well described by the Weibull distribution. To evaluate whether a single Weibull scaling law can explain breakdown results for all the different surfaces, we notice that, for type \(A\), we can fit all the cumulative probability distributions with the same value \(\beta = 52\),

Figure 3. Panels (a) and (b) show \(I-V\) characteristics of, respectively, type \(B\) devices with \(S = 215 \times 195 \mu m^2\) (a), and type \(A\) devices with \(S = 215 \times 195 \mu m^2\) (blue curves), \(S = 175 \times 150 \mu m^2\) (red curves) and \(S = 125 \times 115 \mu m^2\) (black curves) (b). Panels (c) and (d) show the \(I-V\) curves in logarithmic scale for the two types of devices and areas \(S = 215 \times 195 \mu m^2\) (black curves in (c) (d)) and \(S = 175 \times 150 \mu m^2\) (red curves in (d)).
Figure 4. Panel (a) shows histogram plots of the breakdown field for different populations of test devices as specified in the legends. The panels in (b) and (c) show the cumulative probability for type A devices for different surface areas (dots are experimental data, and the continuous line is a fit to the Weibull distribution). The plot in (d) is a fit to the cumulative probability for type B devices ($S = 215 \times 195 \, \mu m^2$) to the Weibull distribution.

We notice that $\beta = 52$—estimated from the fit in figures 4(b) and (c)—is comparable to values found for thermally grown thin SiO$_2$ films, and it is compatible with failure of the devices due to surface roughness [23] probably being transferred to the dielectric film from the Ti/Au substrate. This quantitative analysis make it possible to state that electron-beam evaporated SiO$_2$, directly coated by a metallic layer without exposure to air, has an essentially identical quality to that of thermally grown oxide. A similar analysis of $P$ for type B devices, gives a $\beta = 3.3$, i.e. a much higher dispersion of breakdown field (see figure 4(d)). This small value for $\beta$ in type B devices quantifies the much larger statistical spread of the oxide properties in these devices. Since the only difference between type A and B devices is the fabrication step of
the SiO$_2$/Ti interface, we conclude that exposure of the SiO$_2$ to air is indeed the cause for the poor insulating qualities. Indeed it is well known that SiO$_2$ is a hygroscopic material that easily absorbs humidity in air. The humidity absorbed can affect the composition of the entire layer providing paths for the leakage current, and creating weak spots at which breakdown occurs even at low voltages.

5. Conclusions

In conclusion, we have briefly reviewed transport in double-gated bilayer and trilayer graphene devices. Motivated by the need for large electric fields, we have conducted a statistical study of the breakdown field for over 100 top-gated structures fabricated in different conditions and with different surface areas. Adopting a failure analysis based on the Weibull distribution, we show that the most reliable top gates are obtained when depositing in SiO$_2$/Ti/Au without breaking the vacuum. Electron-beam SiO$_2$ layers evaporated in these ways have insulating characteristics as good as those of thermally grown SiO$_2$ layers.

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